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**10/ 824,219****INFORMATION DISCLOSURE STATEMENT  
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(Use several sheets if necessary)

Applicant(s): **Kawasaki et al.**Filing Date: **April 13, 2004**Group Art Unit: **2154****U.S. PATENT DOCUMENTS**

*EXAMINER INITIAL	DOCUMENT NUMBER							DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
<i>NZ</i>	4	4	9	1	9	0	7		Koeppen et al.			
	4	6	2	6	9	8	5	12/86	Briggs	395	800-4	
	4	6	4	9	5	1	1	3/87	Gdula	711	106	
	4	6	7	0	8	3	8	6/87	Kawata	714	38	
	4	7	9	4	5	2	4	12/88	Carberry et al.	712	32	
	4	8	7	0	5	6	2	9/89	Kimoto et al.	711	167	
	4	9	1	8	6	5	0	4/90	Wolf	710	129	
	4	9	3	5	8	6	7	6/90	Wang et al.	711	217	
	4	9	7	5	5	9	3	12/90	Kurakazu et al.	327	141	
	4	9	8	4	1	9	5	1/8/91	Nakamura et al.	364	200	6/2/88
	5	1	2	4	0	8	4	6/3/92	Begun			
	5	1	5	5	8	1	9	10/92	Watkins et al.	395	800-36	
	5	1	7	5	8	4	1	12/92	Magar et al.	711	211	
	5	2	2	7	8	6	3	07/93	Bilbrey et al.	348	578	
	5	2	7	0	8	9	8	12/93	Elms et al.	361	96	
	5	3	4	1	1	7	2	8/94	Nio et al.	348	441	
	5	3	5	3	4	2	4		Partovi et al.			
	5	3	8	6	5	7	3	1/95	Okamoto	395	733	5/93
	5	3	8	8	8	4	1	2/95	San et al.	273	435	1/92
	5	3	9	8	0	4	8	3/95	O'Mahony	345	212	
	5	4	2	6	7	4	4	6/95	Sawase et al.	712	228	
	5	4	2	6	7	6	9	6/95	Pawluski	395	500	8/93
	5	4	3	0	6	8	8	07/95	Takasugi, Atsushi	365	233	
	5	4	6	9	5	4	4		Aatresh et al.			
	5	4	9	3	6	5	6	2/96	Tsukamoto	395	280	8/90
	5	5	0	6	9	7	3		Okazawa et al.			
	5	5	3	0	8	9	0		Moore et al.			
	5	6	5	9	7	9	7	8/97	Zandveld et al.	395	842	6/92
<i>NZ</i>	5	5	7	4	8	7	6	11/96	Uchiyama et al.	711	5	

	5	8	7	8	2	6	9	3/99	Eitrheim et al.	712	42	
<b>FOREIGN PATENT DOCUMENTS</b>												
	DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
NE	0	2	1	2	6	4	0	04/87	EUROPE- Kelda et al.			YES NO
	0	3	4	6	9	1	7	12/89	EUROPE	G06F	13/28	X
	0	5	0	6	5	9	4	9/92	EUROPE	G06F	3/12	X
	0	5	2	3	7	6	4	1/93	EUROPE	G06F	13/28	X
	0	5	8	8	6	0	7	3/94	EUROPE	G06F	15/78	X
NE	0	6	2	4	8	4	4	11/94	EUROPE	G06F	12/08	X
<b>OTHER DOCUMENTS</b> (Including Author, Title, Date, Pertinent Pages, Etc.)												
NE	IEEE Journal of Solid-State Circuits, Vol. 26, No. 11, November 11, 1991, pp. 1586-92, "A 0.5W 64-Kilobyte Snoopy Cache Memory with Pseudo Two-Port Operation" by Kobayashi et al.											
	Proceedings, IEEE 1993 Custom Integrated Circuits Conference, May 9, 1993, pp. 25.21-25.24, "A High Performance/Low Power K-byte 4-Way Set Associative Integrated Cache Memory," by Nguyen et al.											
NE	IBM Technical Disclosure Bulletin, November 1989, Vol. 32, No. 6A, pp. 246-248, "Method of Communication Between a PC and a 68000-Based System Using Parallel Ports."											
EXAMINER <i>N. S. Hardy</i>									DATE CONSIDERED <i>6/27/05</i>			
*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.												